Subject code: 24EC11RC04 R-24 Date of Exam: 30/06/2025

Gayatri Vidya Parishad College of Engineering for Women
(Autonomous)

I B. Tech. - II Semester Regular Examinations, June-2025

Elements of Electronics Engineering
(common to CSE & IT)

Detailed Scheme of Valuation

UNIT-I

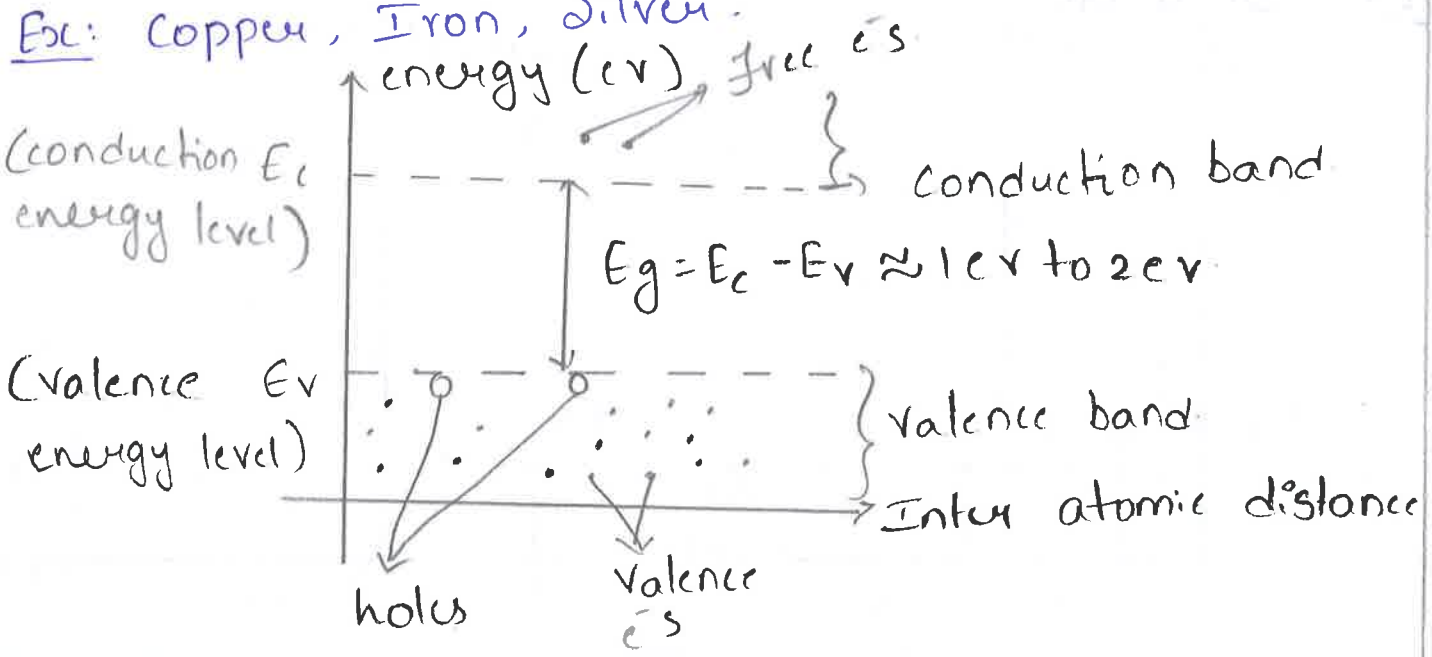
1)a) Difference between conductors, insulators and semiconductors based on energy bands [7M]

Ans Conductors:-

(i) At T=0K, more number of free e's are available in conduction band. Hence material exhibits conductor property.

(ii) At T=300K, more number of free electrons are available in conduction band. Hence, exhibits conductor property

Ex: Copper, Iron, Silver.

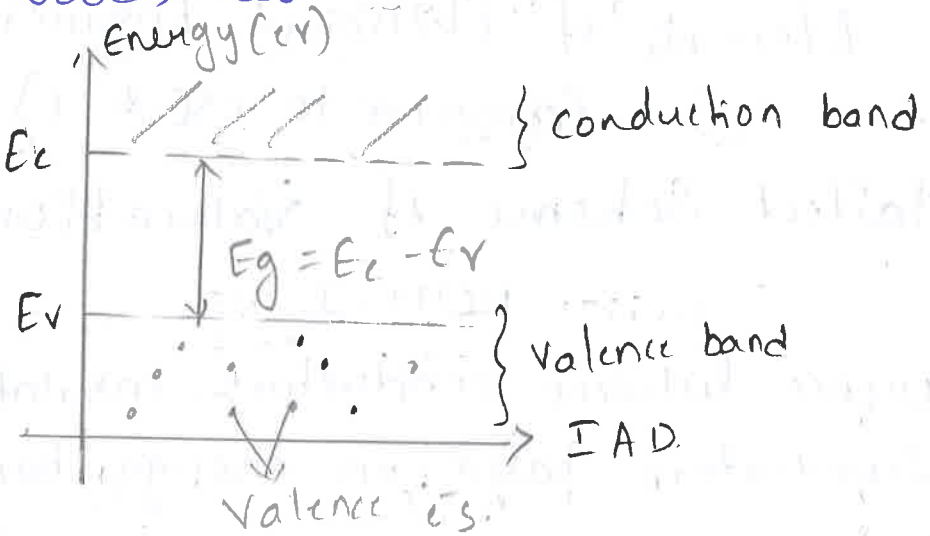


Insulator:-

(i) At T=0K, no free electrons in conduction band. Hence, it exhibits insulator property.

(ii) At T=300K, no free es in conduction band.

Ex: Carbon, wood, neon

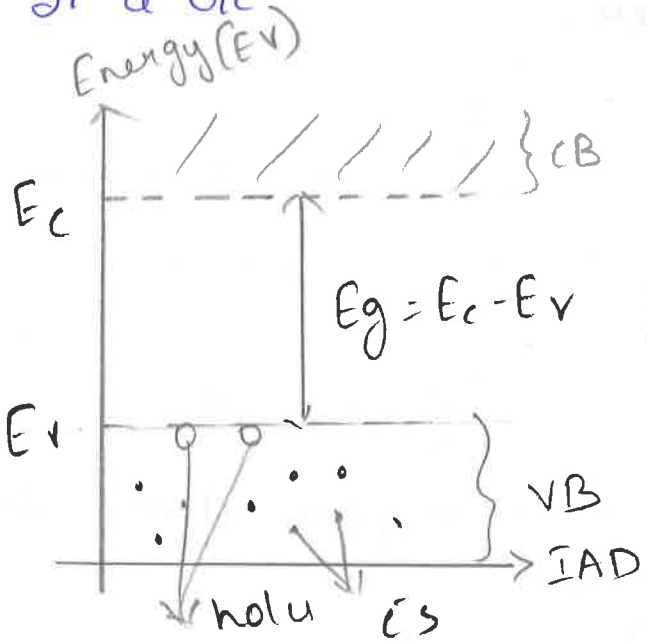


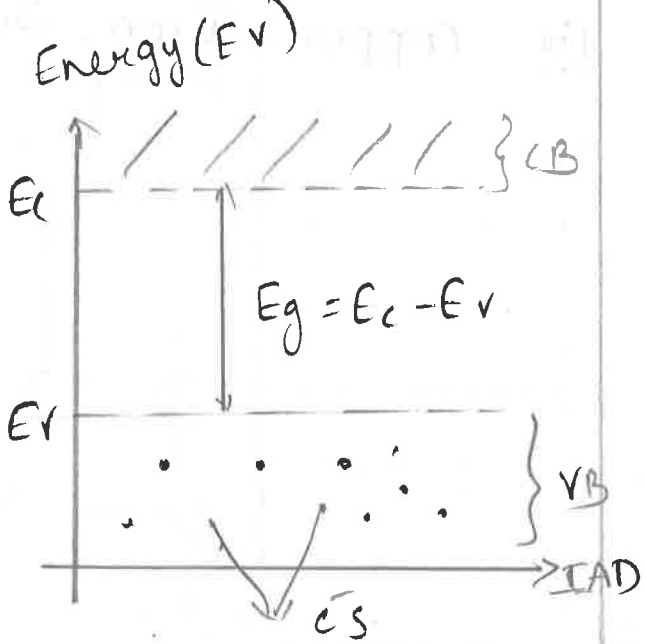
Semiconductor:

(i) NO free es are available in conduction band at temperature T=0K. The Semiconductor acts as a Insulator

(ii) Free es are available in conduction band at temp. T=300K. It acts as a conductor

Ex: Si & Ge.





1)b) what is the total current in a semiconductor under both drift and diffusion mechanisms? [1M]

Ans Drift current: The current due to drift or movement of free electrons in a semiconductor under the influence of external voltage or electric field is called drift current.

* It is observed in both semiconductors and conductors.

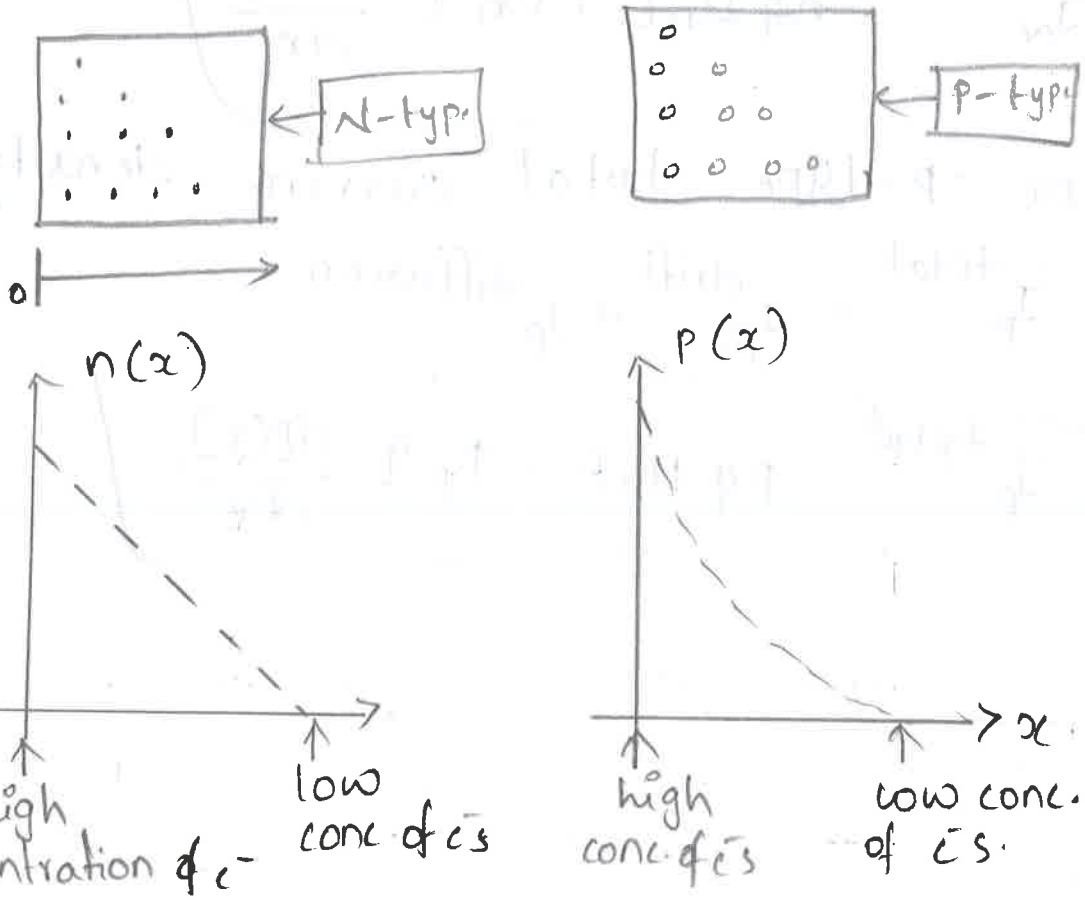
* Drift current density due to holes is given by

$$J_p^{drift} = p q \mu_p E \quad Amp/m^2$$

* Drift current density due to electrons is given by

$$J_n^{drift} = n q \mu_n E \quad Amp/m^2$$

Diffusion current :-



- The current due to transfer of charge carriers from high concentration region to low concentration region in a non-uniform doped semiconductor is called diffusion current)
- Diffusion current density due to electrons

$$J_n^{diffusion} = +D_n q \frac{dn(x)}{dx}$$

- Diffusion current density due to holes

$$J_{diffusion}^{p} = -D_p q \frac{dp(x)}{dx}$$

- For N-type total current density

$$J_N^{total} = J_N^{drift} + J_N^{diffusion}$$

$$J_N^{total} = nq\mu_n E + D_n q \frac{dn(x)}{dx}$$

- For P-type total current density

$$J_p^{total} = J_p^{drift} + J_p^{diffusion}$$

$$J_p^{total} = pq\mu_p E - D_p q \frac{dp(x)}{dx}$$

2)a) Derive an expression for carrier concentration in intrinsic semiconductors [7M]

In intrinsic semiconductor, the electron concentration is equal to holes concentration i.e. $n = P$

According to law of mass action

$$n \times P = n_i^2$$

Where $n = N_c e^{-(E_c - E_F)/KT}$

$$P = N_v e^{-(E_F - E_v)/KT}$$

$$n_i^2 = N_c e^{-(E_c - E_F)/KT} \times N_v e^{-(E_F - E_v)/KT}$$

$$= N_c N_v e^{-(E_c - E_F + E_F - E_v)/KT}$$

$$= N_c N_v e^{-(E_c - E_v)/KT}$$

But $E_g = E_c - E_v$

$$n_i^2 = N_c N_v e^{-E_g/KT}$$

$$\boxed{n_i = \sqrt{N_c N_v e^{-E_g/KT}}}$$

But $N_c = 2\left(\frac{2\pi m_n^* KT}{h^2}\right)^{3/2}$

$N_v = 2\left(\frac{2\pi m_p^* KT}{h^2}\right)^{3/2}$

$$n_i = 2\left(\frac{2\pi K}{h^2}\right)^{3/2} (m_n^* m_p^*)^{3/4} (T)^{3/2} e^{-E_g/2KT}$$

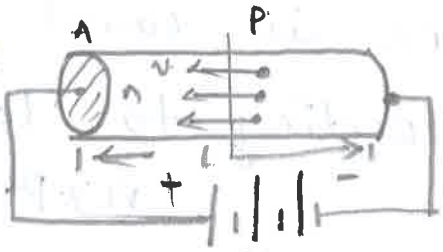
$A \rightarrow$ constant

$$\therefore \boxed{n_i = A T^{3/2} e^{-E_g/2KT}}$$

2)b) How does conduction occur in conductors, Semiconductors, and insulators? [7M]

Sol Conductivity of conductors:-

Consider a conductor of length l meters and cross-sectional area A Square meters.



- Let the number of free electrons available per m^3 of the conductor material i.e electron density be n and E be the applied electric field.
- Due to the applied electric field, let axial drift velocity of the es be v mts/second.
- The force F on the particle of charge q when an electric field E is given as $\boxed{F = qE}$

also $\boxed{F = ma}$

drift velocity $v = a \times \tau = \frac{eE}{m} \times \tau$.

current in a conductor $I = \frac{dq}{dt} = envA$

The current density $J = \frac{I}{A} = env$ and also

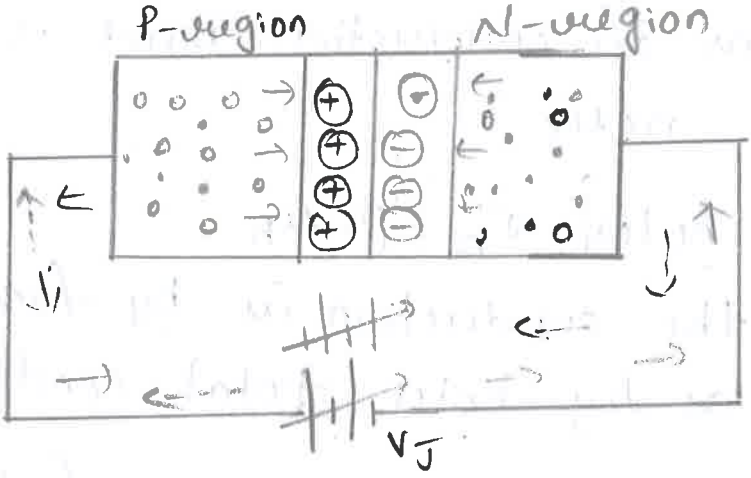
$\boxed{J = \sigma E}$

Electrical conductivity of the material is given as $\boxed{\sigma = \frac{ne^2\tau}{m} = ne\mu_e}$

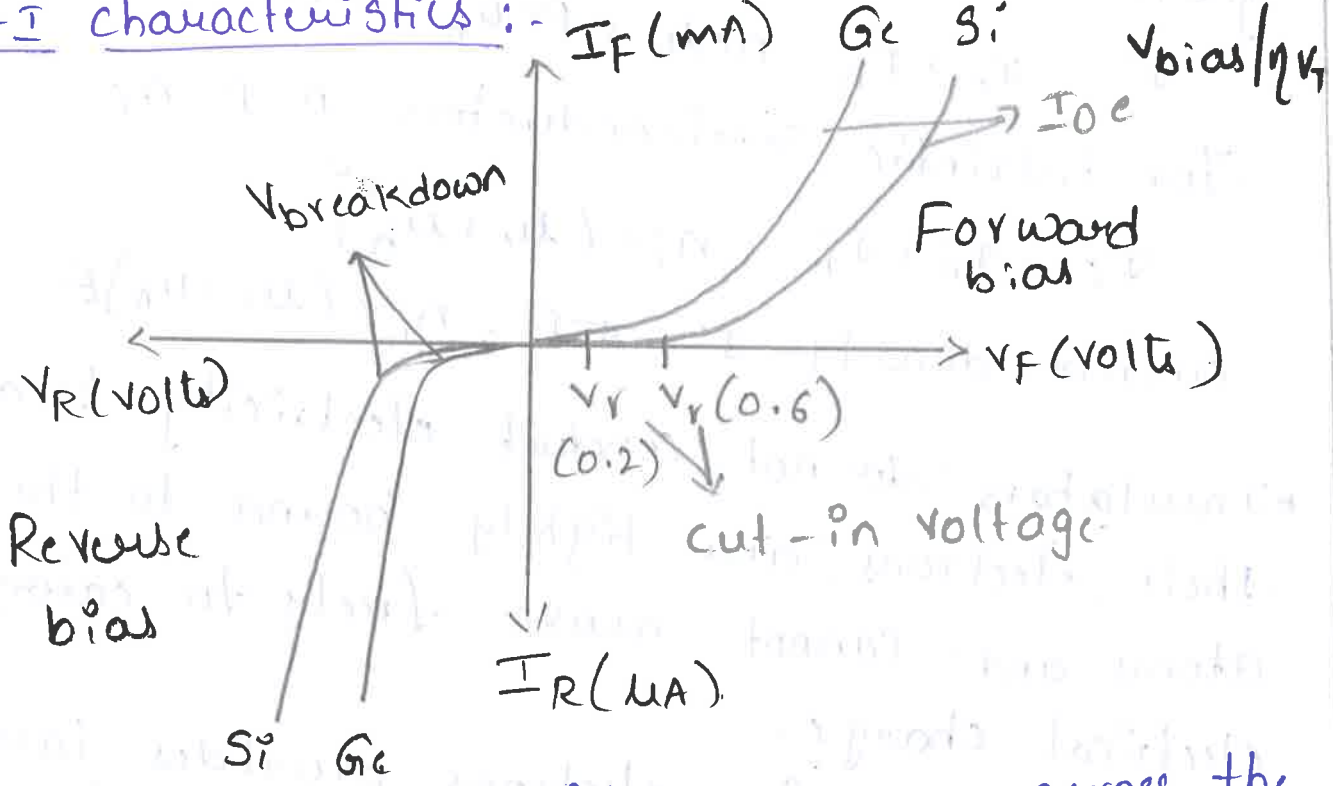
UNIT-II

3)a) Sketch and explain the V-I characteristics of a PN junction diode. [7M]

Ans



V-I characteristics :-



cut-in voltage: The forward voltage across the diode at which the diode starts conduction of its maximum current is called cut-in voltage or knee voltage (V_r)

For Ge $V_r \longrightarrow 0.2$ to $0.3V$

Si $V_r \longrightarrow 0.6$ to $0.7V$.

conductivity of Semiconductors :- Insulators.

- The conductivity of σ_e of the semiconductor due to electrons in conduction band is given as

$$\sigma_e = n e \mu_e$$

Due to holes $\sigma_h = p e \mu_h$.

- In SC's the conduction is by free electrons as well as by holes, total conductivity σ is given as

$$\sigma = \sigma_e + \sigma_h = n e \mu_e + p e \mu_h = e(n\mu_e + p\mu_h)$$

For intrintic semiconductors $n = p = n_i$

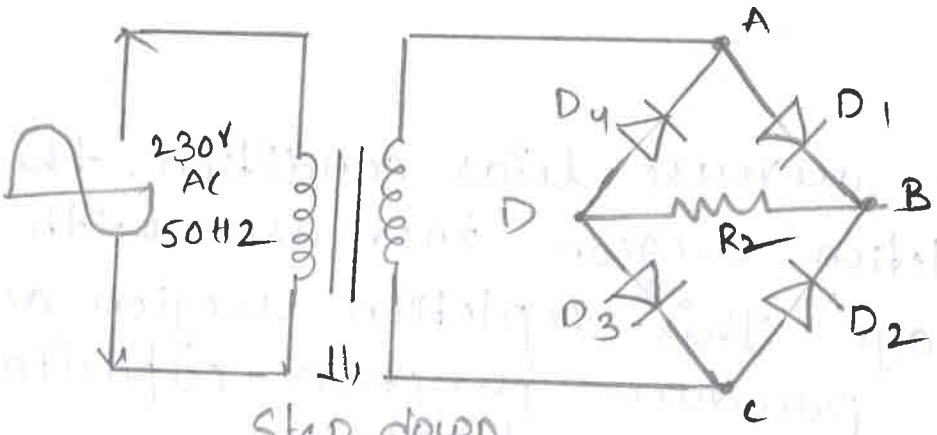
$$\sigma_i = \sigma_n + \sigma_h = n_i e(\mu_e + \mu_h)$$

current density $J = \sigma E = n_i e(\mu_e + \mu_h) E$

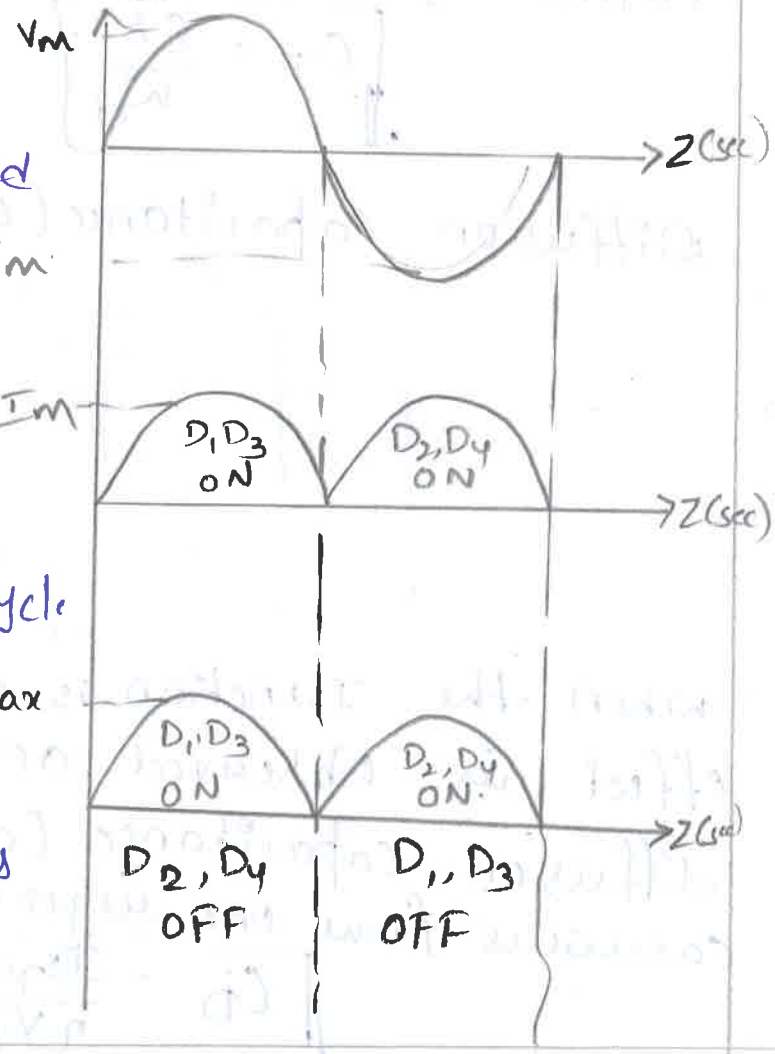
- Insulators do not conduct electricity because their electrons are tightly bound to their atoms and cannot move freely to carry an electrical charge.
- This lack of free electrons provides large band gap between the valence band and conduction band.

Breakdown voltage:- The reverse voltage across the diode for which the diode to maintain constant output voltage. This voltage is also called Avalanche Breakdown.

3)b) Draw the circuit of a Bridge rectifier without filter and explain its operation. [7M]



x(t)

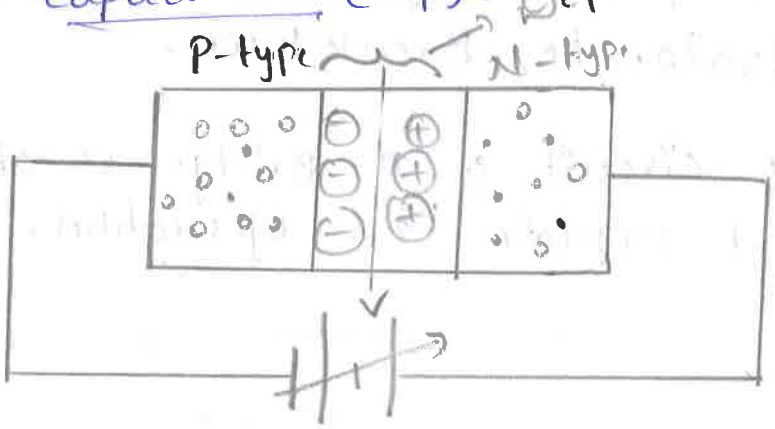


Case I: During positive cycle Diodes D_1, D_3 ON, operated in forward bias condition, D_2, D_4 OFF operated reverse bias condition.

Case II: During negative cycle Diodes D_2, D_4 is in forward bias acts as ON D_1, D_3 is in reverse bias acts as OFF.

4)a) Differentiate between transition capacitance and diffusion capacitance. [7M].

1. Transition capacitance (C_T): Depletion region

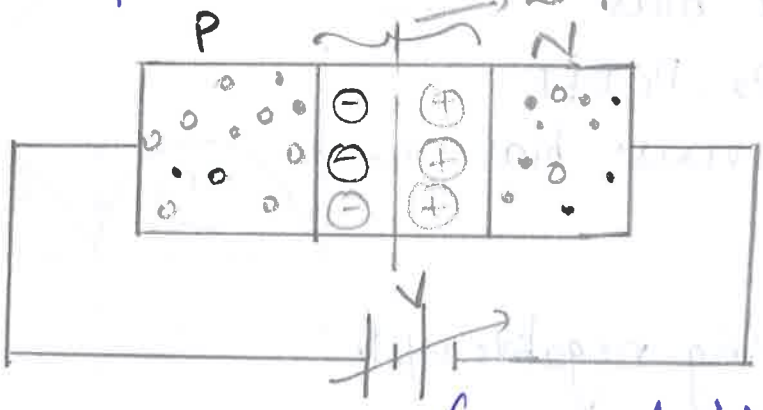


- Under reverse bias condition, the width of depletion region increases with increase in voltage. This depletion region acts as dielectric produces junction capacitance called Transition capacitance.

$$C_T = \frac{\varepsilon A}{W_d}$$

$W_d \rightarrow$ depletion width.

Diffusion capacitance (C_D). Depletion region



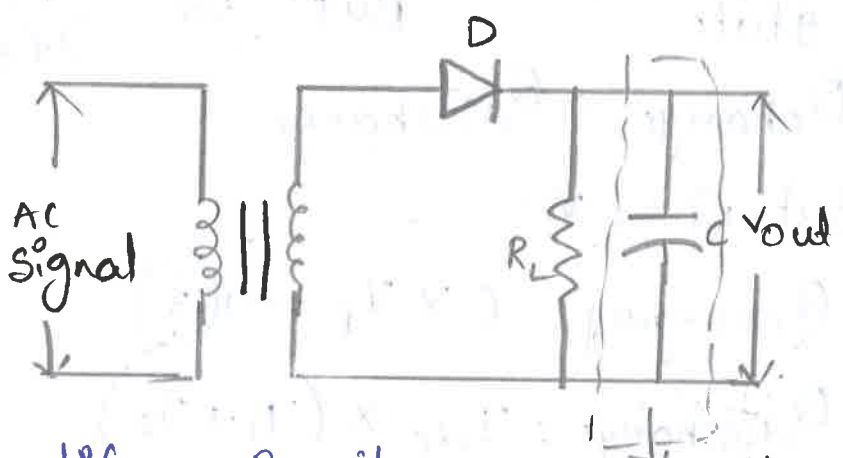
When the Junction is forward bias a capacitance effect is observed across the PN diode called diffusion capacitance (due to diffusion of charge carriers from one region to other)

$$C_D = \frac{I \tau}{\eta V_T}$$

$\tau \rightarrow$ mean lifetime

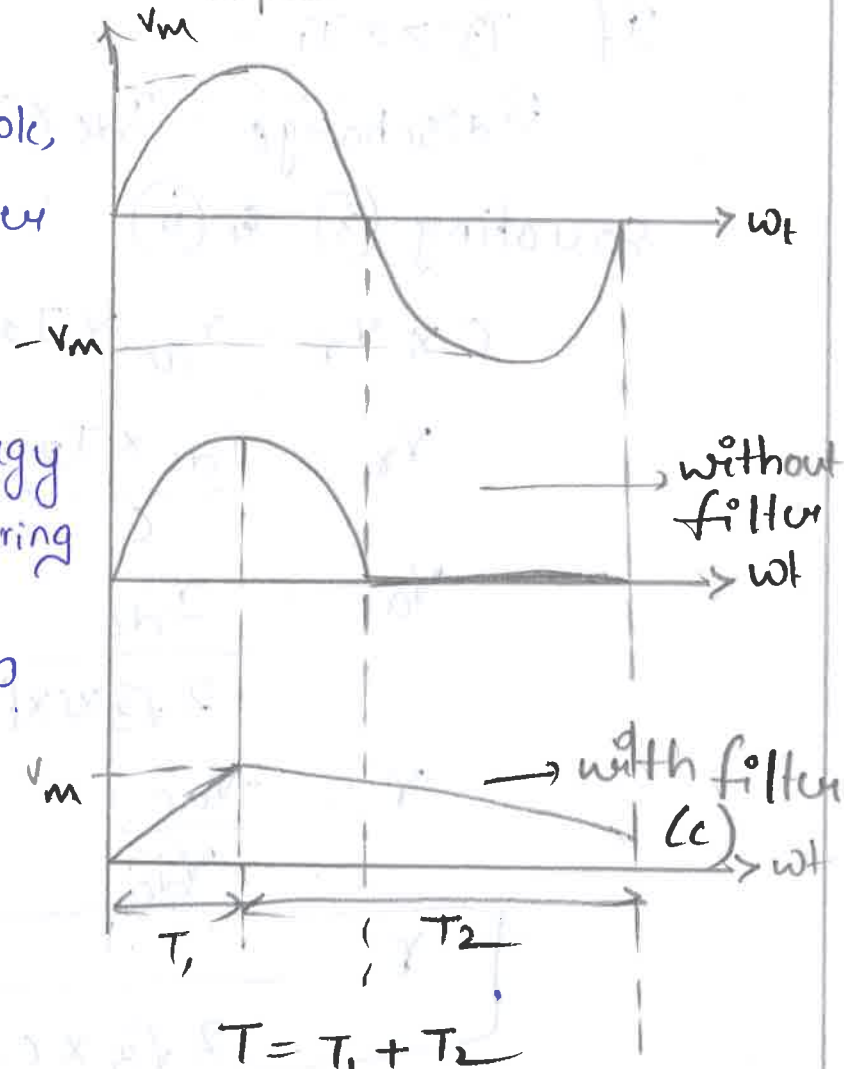
4)b) What is the role of a capacitor filter in a halfwave rectifier circuit with the help of circuit diagram?

Ans. Half-wave rectifier with capacitor filter :-



capacitor filter

- In rectifier circuits, a capacitor filter reduces voltage ripple, providing a smoother DC output.
- The capacitor acts as a temporary energy storage, charging during the diodes on-time and discharging to maintain voltage during off-time.



$T = T_1 + T_2$

The ripple factor of a HWR with c filter is defined as the ratio of ac voltage to dc voltage

$$\text{i.e. } \gamma = \frac{V_{ac}}{V_{dc}} = \frac{I_{ac}}{I_{dc}} \rightarrow (1)$$

At steady state But $V_{ac} = \frac{V_r}{2\sqrt{3}} \rightarrow (2)$

$$Q_{charge} = Q_{discharge}$$

But $Q = CV$

$$\therefore Q_{charging} = C \times V_r \rightarrow (3)$$

$$Q_{discharge} = I_{dc} \times (T_1 + T_2)$$

If $T_2 >> T_1$

$$Q_{discharge} = I_{dc} \times T_2 \rightarrow (4)$$

Equating (3) & (4)

$$C \times V_r = I_{dc} \times T_2$$

$$V_r = \frac{I_{dc} \times T_2}{C}$$

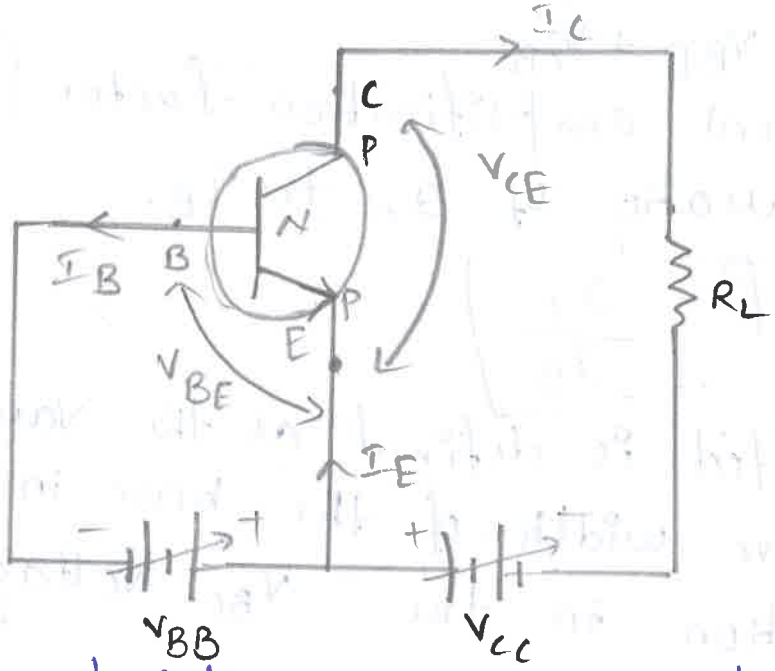
$$V_{ac} = \frac{I_{dc}}{2\sqrt{3} \times C \times f}$$

$$\gamma = \frac{V_{ac}}{V_{dc}}$$

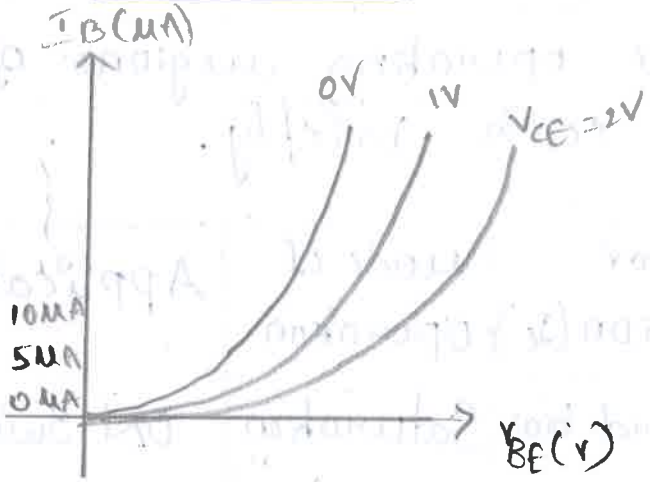
$$\boxed{\gamma = \frac{1}{2\sqrt{3} \times C \times f \times R_L}}$$

∴ The ripple factor depends on the value of capacitance.

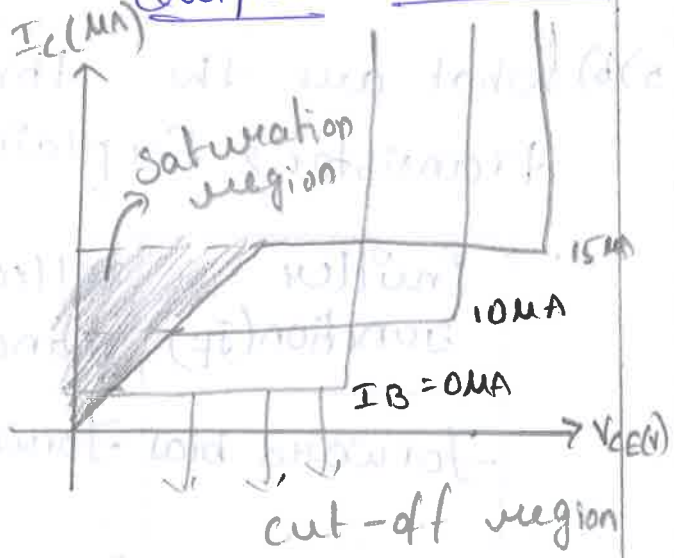
5)a) Draw the circuit and explain the operation of a BJT in CE configuration [7M]



Input characteristics



Output characteristics



- For a CE, as the emitter junction J_E is operated in forward bias it exhibits forward bias characteristics. In this case V_{BE} increases I_B current also varied while keeping output voltage V_{CE} is constant.
- As the collector junction J_c is operated in

Reverse bias condition it exhibits reverse bias characteristics. In this case V_{CE} increases I_C is also varied where I_B remains constant.

$$V_{CE} = V_{BE} + V_{CB}.$$

- The current amplification factor β is defined as the ratio of I_C to I_B

$$\beta = \frac{I_C}{I_B}$$

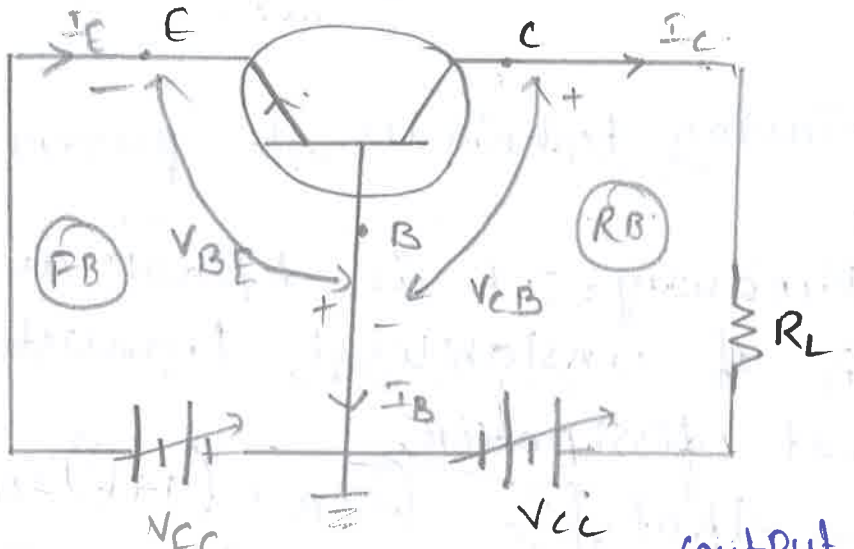
- Early effect is defined as the variation in the effective width of the base in BJT due to variation in the V_{BC} voltage.

5)b) What are the three operating regions of a transistor? Explain each briefly.

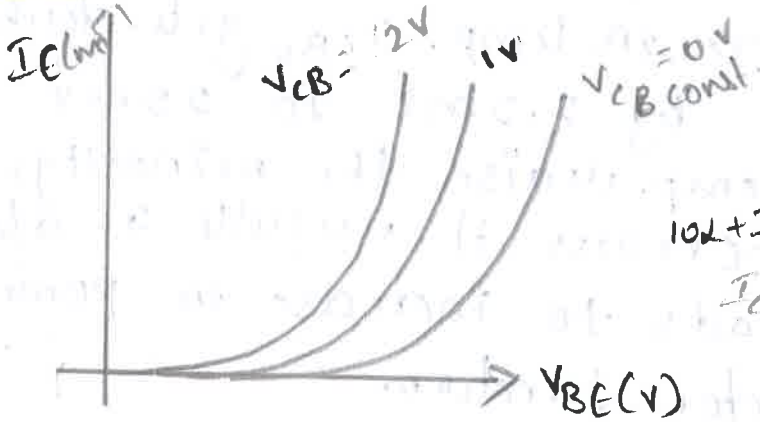
Emitter Junction(J_E)	collector Junction(J_C)	Mode of operation	Application
Forward bias	Forward bias	Saturation	ON Switch
FB	Reverse bias	Active	Amplifier
RB	FB	Inverse active	Inverse of amplifier
RB	RB	cut off	OFF Switch

6)a) Analyze the input and output characteristics of a BJT in a common Base (CB) configuration and discuss the effect of base width modulation [7M]

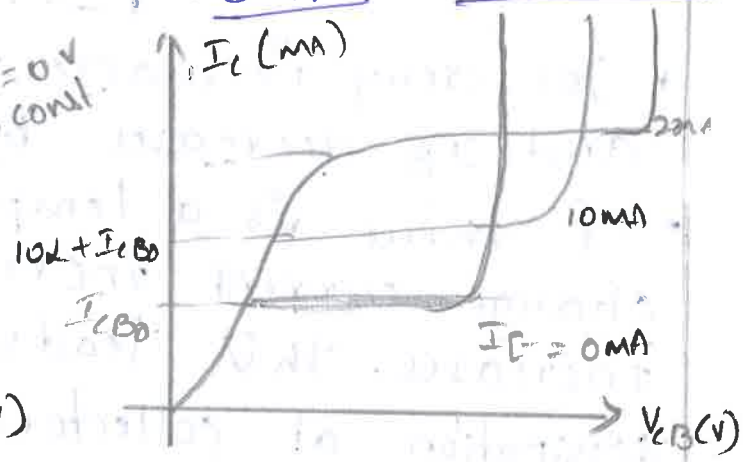
Ans



Input



Output characteristics



- In this configuration I_B current increases then the I_E also increases it results effective depletion width of the base is increases when V_{BE} increases. (Forward bias condition)
- If the output is operated in RB condition, then the V_{CB} increases, then the junction potential at the collector is also increases then the depletion width at the collector increases.

∴ The collector current I_C is given by

$$I_C = \alpha I_E + I_{CBO}$$

6)b) How do biasing techniques to prevent thermal Runaway? [7M]

Thermal Runaway: It is defined as the self destruction of unstabilized transistor due to excess heat dissipation.

We know that $I_C = \beta I_B + (1+\beta) I_{CBO}$

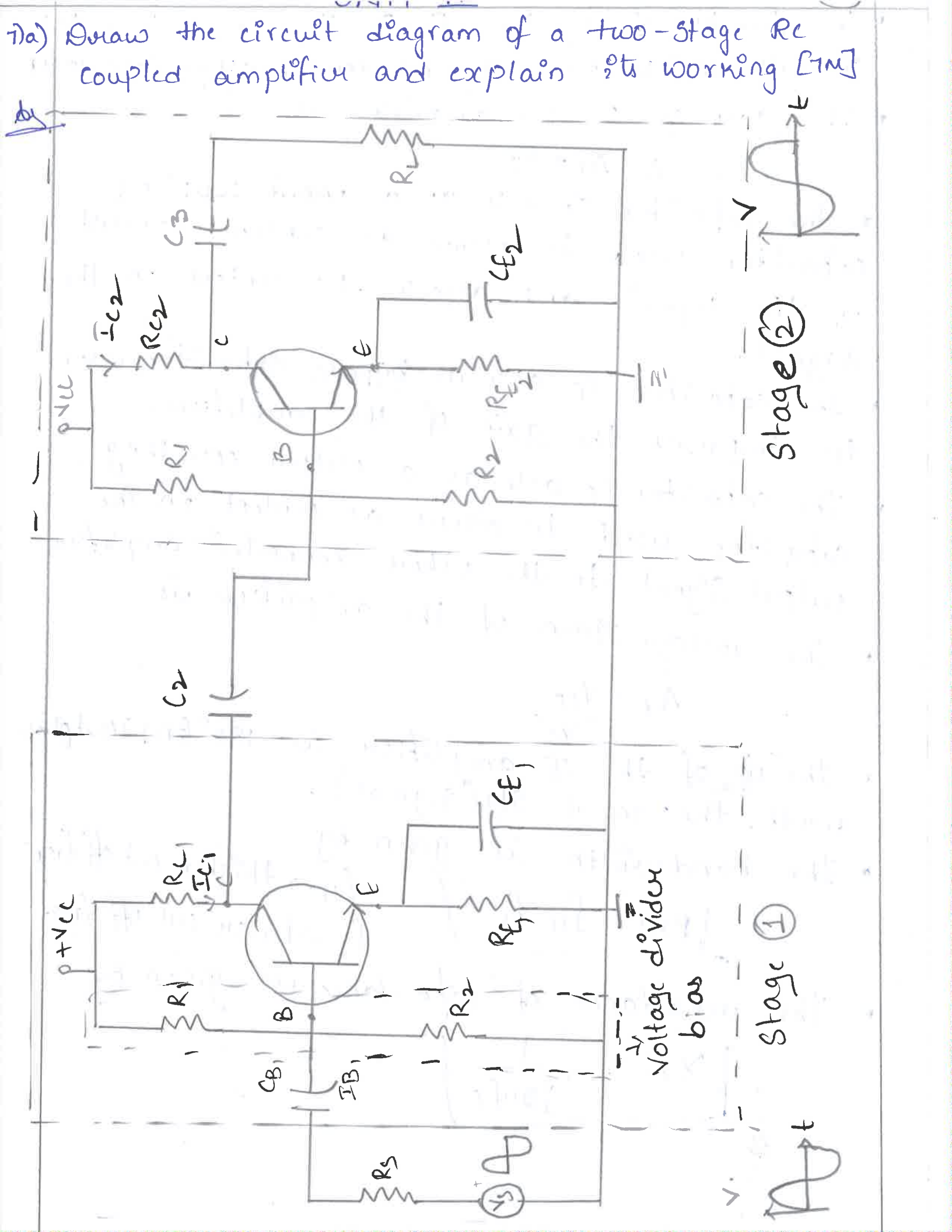
- For every 1°c raise in temp. I_{CBO} gets doubled and I_B decreases by 2.5mv to 25mv.
- If there is a temp. raise the minority charge current increases it results I_C also increases. This leads to increase in power dissipation at collector junction.

Bias Stabilization Techniques:

1) Base bias or fixed bias
2) Emitter bias
3) collector feedback
4) Voltage divider bias or Self bias

- By Stabilizing the operating point against temperature variations biasing techniques can be used to prevent thermal runaway in transistors.

7)a) Draw the circuit diagram of a two-stage RC coupled amplifier and explain its working [7M]



* The function of resistors R_1, R_2, R_C & R_E is to protect stability of Q point against temperature variations
* The gain of 2-stage amplifier is

$$A = A_1 * A_2$$

* The capacitor C_B acts as a input coupling capacitor used to allow ac content present in the signal and rejects DC content in the signal.
* The capacitor C_E acts as bypass capacitor used to improves the gain of the amplifier.
* The capacitor C_C acts as a output coupling capacitor used to allow ac content in the output signal to the other connected amplifier
* The voltage gain of the amplifier is

$$A_V = \frac{V_{CE}}{V_S}$$

* The o/p of the CE amplifier is 180° (or) out phase with the input Sig (Signal).
* The band width is given by

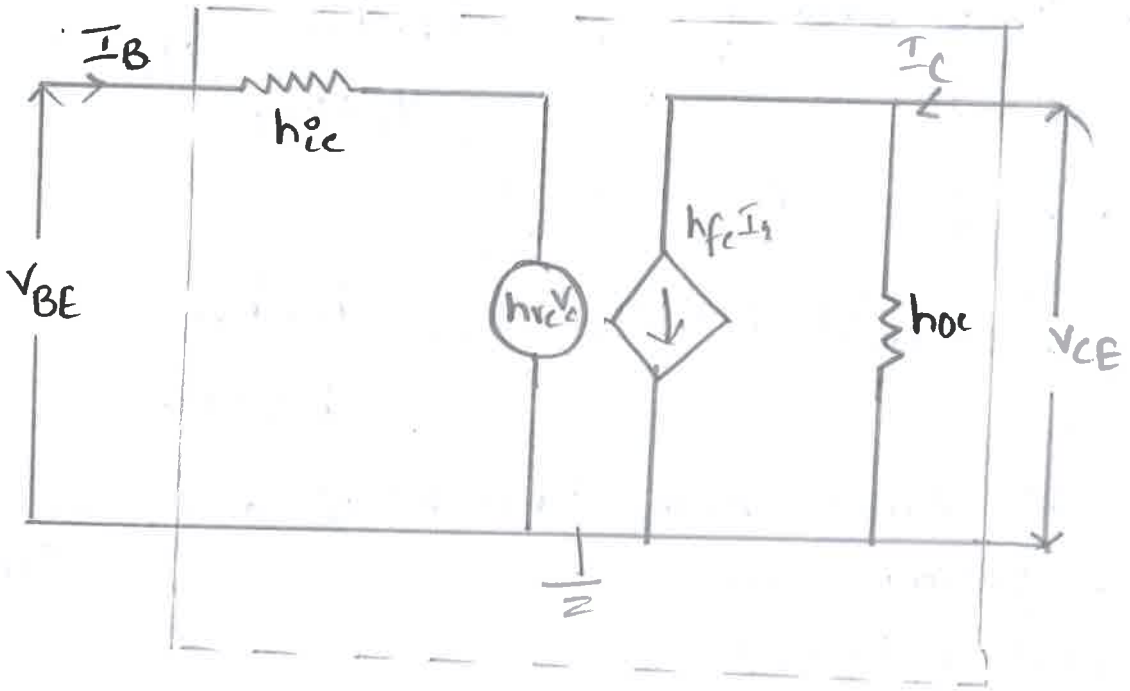
$$BW = f_H - f_L$$

f_H → Higher cut-off freq
f_L → Lower cut-off freq.

* The reactance of capacitance is given by

$$X_C = \frac{1}{j2\pi fC}$$

7)b) Derive an expressions for voltage gain, current gain, input and output resistance of a CE amplifier using h-parameters. [7M]



$$V_{BE} = h_{ie} I_B + h_{re} V_{CE}$$

$$I_C = h_{fe} I_B + h_{oe} V_{CE}$$

where $h_o = \frac{1}{R_o}$ or $\frac{1}{Z_o}$

$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right| V_c = \text{constant}.$$

$$h_{re} = \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right| I_B = \text{constant}$$

$$h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right| V_{CE} = \text{constant}$$

$$h_{oe} = \left.\frac{\Delta I_C}{\Delta V_{CE}}\right| I_B = \text{constant}$$

current gain $A_I = \frac{-h_{fe}}{1+h_{oe}Z_L}$ $(Z_L = R_L)$

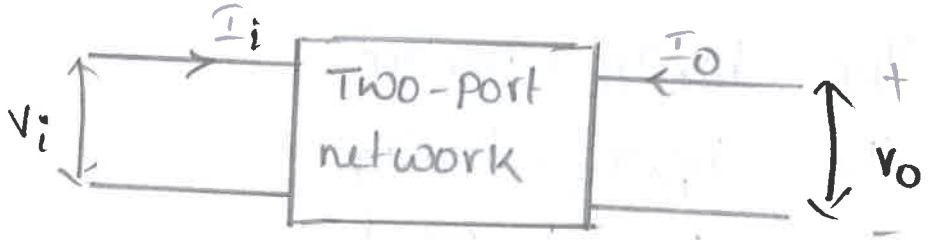
Input Impedance $Z_i = h_{ie} - \frac{h_{fe}\,h_{re}}{Y_L + h_{oe}}$ $\left[Y_L = \frac{1}{Z_L} = \frac{1}{R_L}\right]$

voltage gain $A_V = A_I \frac{Z_L}{Z_i}$

Output admittance $Y_o = h_{oe} - \frac{h_{fe}\,h_{re}}{h_{ie} + R_S}$.

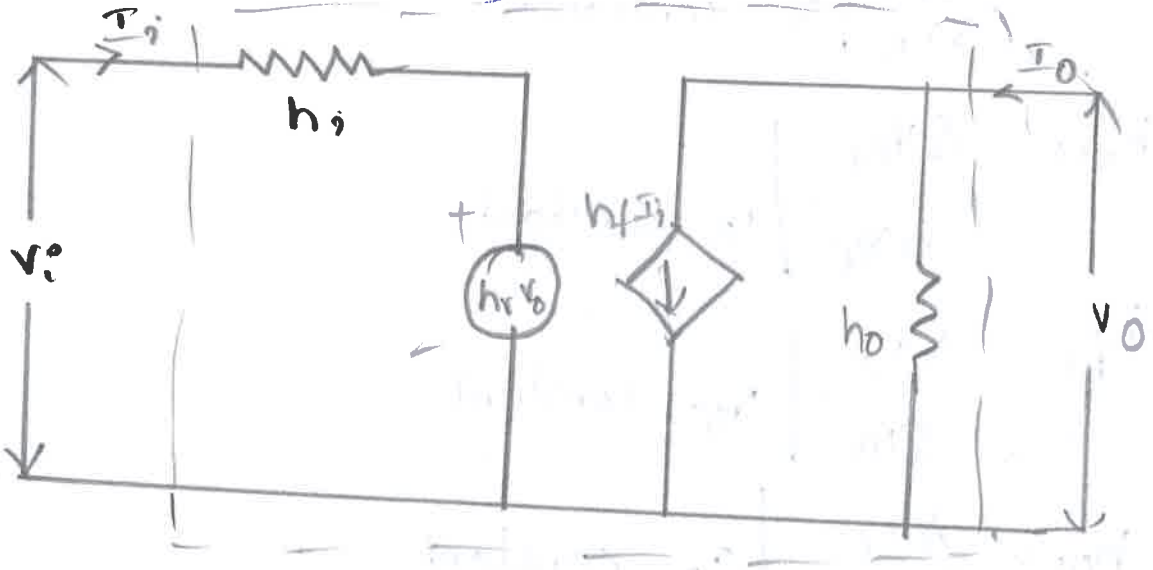
8)a) Explain the small signal model of a transistor using h-parameters [7M]

A) Two-port network:



$V_i = f(I_i, V_o)$

$I_o = f(I_i, V_o)$



Definitions of H-parameters:-

$h_i = h_{11} = \frac{V_i}{I_i} \Big|_{V_o \text{ (const)}}$ → Input resistance

$h_r = h_{12} = \frac{V_i}{V_o} \Big|_{I_i \text{ const.}}$ → Reverse voltage gain

$h_f = h_{21} = \frac{I_o}{I_i} \Big|_{V_o \text{ const.}}$ → forward current gain

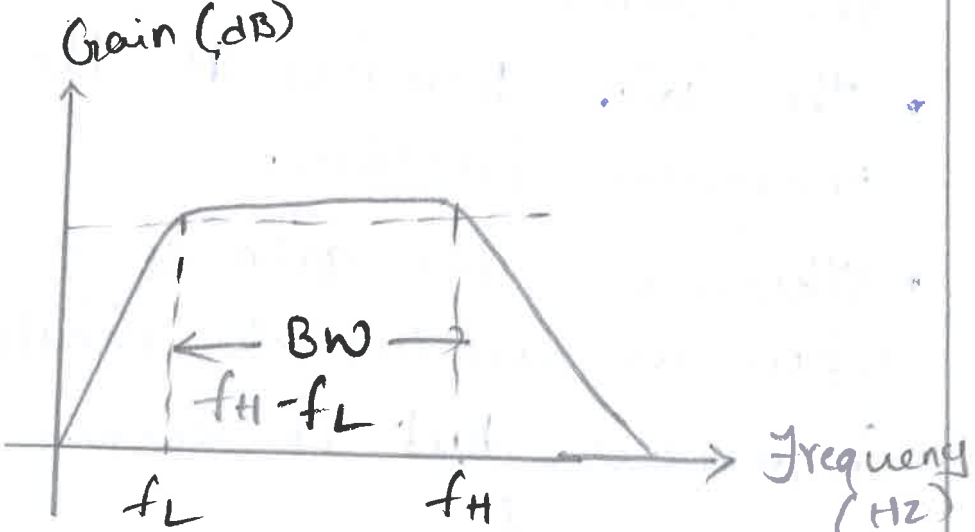
$h_o = h_{22} = \frac{I_o}{V_o} \Big|_{I_i \text{ const.}}$ → output admittance

From the above circuit

$$V_i = h_i I_i + h_r V_o$$

$$I_o = h_f I_i + h_o V_o .$$

8)b) Explain how gain changes in the low, mid, and high frequency ranges in a two-stage amplifier [7M]



- In a two-stage amplifier, gain varies across different frequency ranges due to the behavior of coupling and parasitic capacitances
- At mid-band frequencies, the gain is relatively constant, while at low and high frequencies the gain decreases.
- In the mid-frequency range, coupling capacitors (c) act as open circuits at low frequencies and short circuits at high frequencies, (gain constant.)
- At low frequencies, coupling capacitors (c) exhibit high impedance, acting as a high-pass filter. In this case, gain decreases.
- At high frequencies, parasitic capacitances shunt the signal to ground, reducing the effective load impedance and thus decreasing the gain.
- The gain decreases as the frequency increases further.
- Therefore, the gain of a two-stage amplifier is relatively constant at mid-band frequencies, but it decreases at both low and high frequencies.

9a) Define and explain the JFET parameters.

A) 1) Transconductance (g_m)

2) Input resistance (R_m or R_S or R_{in})

3) Drain to Source resistance (r_d)

4) Amplification factor (μ)

1) Transconductance (g_m): It is defined as the ratio of drain current to the gate to source voltage.

i.e $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ where $V_{DS} \rightarrow$ constant.

$$g_m = \frac{2 I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$

2) Input resistance (R_m): It is defined as the ratio of gate to Source voltage to the gate reverse saturation current.

i.e. $$\boxed{R_{in} = \frac{V_{GS}}{I_{GSS}}}$$

3) Drain to Source resistance (r_d): It is defined as the ratio of change in drain to source voltage to the change in drain current at constant V_{GS} i.e.

$$\boxed{r_d = \frac{\Delta V_{DS}}{\Delta I_D}}$$ where V_{GS} = constant.

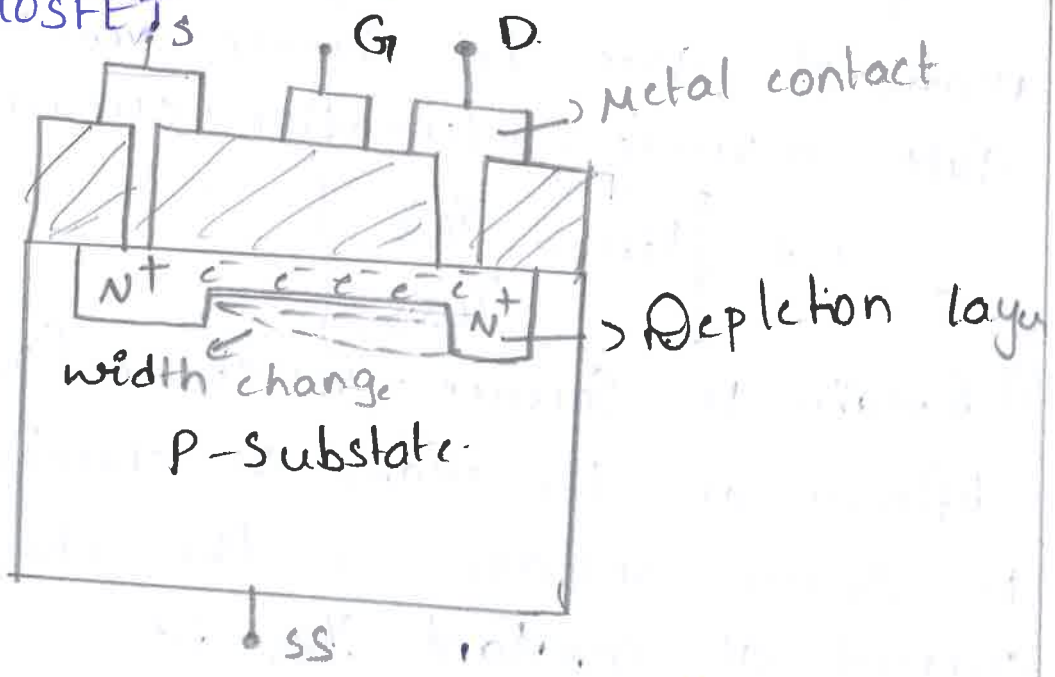
(4) Amplification factor (μ) : It is defined as the ratio of change in drain to source voltage to the change in gate to source voltage at constant drain current

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$ where $I_D \rightarrow$ constant

$$= \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D}$$

$$\mu = g_m \times r_d$$

9)b) Draw and explain the construction of n-channel Depletion MOSFETs



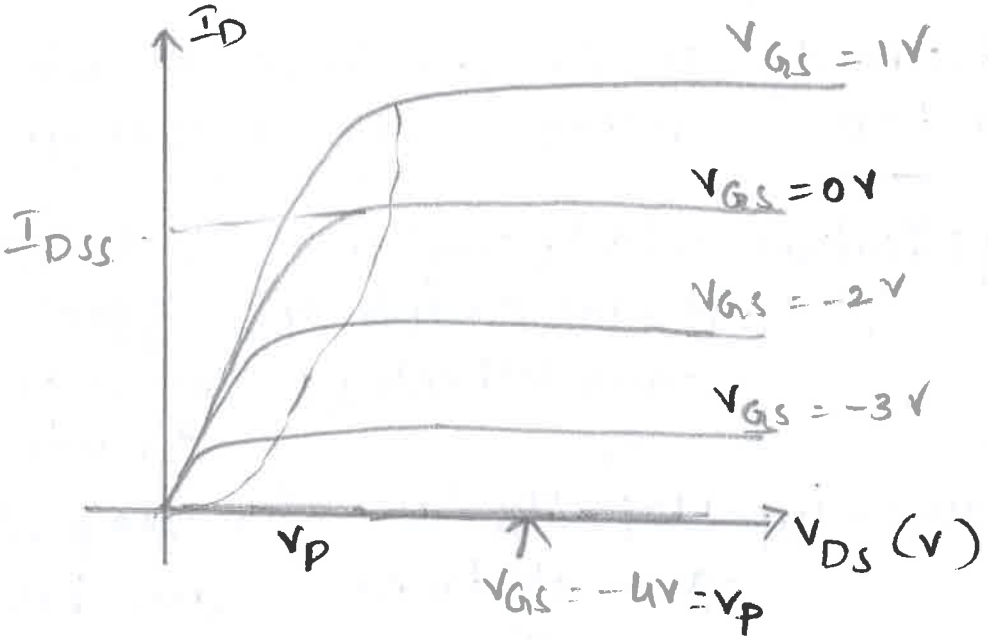
Case I :- If $V_{GS} = 0V$, $V_{DS} = 0V$, the gate voltage should be connected such that the channel width is reduced with increase in V_{GS}.

* V_{DS} should be connected such that the drain current flows from drain to source.

Case 2:

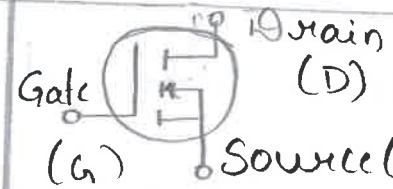
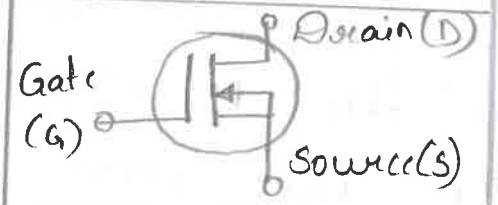
* If $V_{GS} = 0V$, $V_{DS} > 0V$ i.e. there is a variation in V_{DS} voltage then the I_D current increases, the width of depletion layer becomes maximum.

Case 3: when $V_{GS} < 0V$, $V_{DS} = 0V$ then the channel width decreases along the drain terminal In this case $V_{GD} = -V_{GS}$.



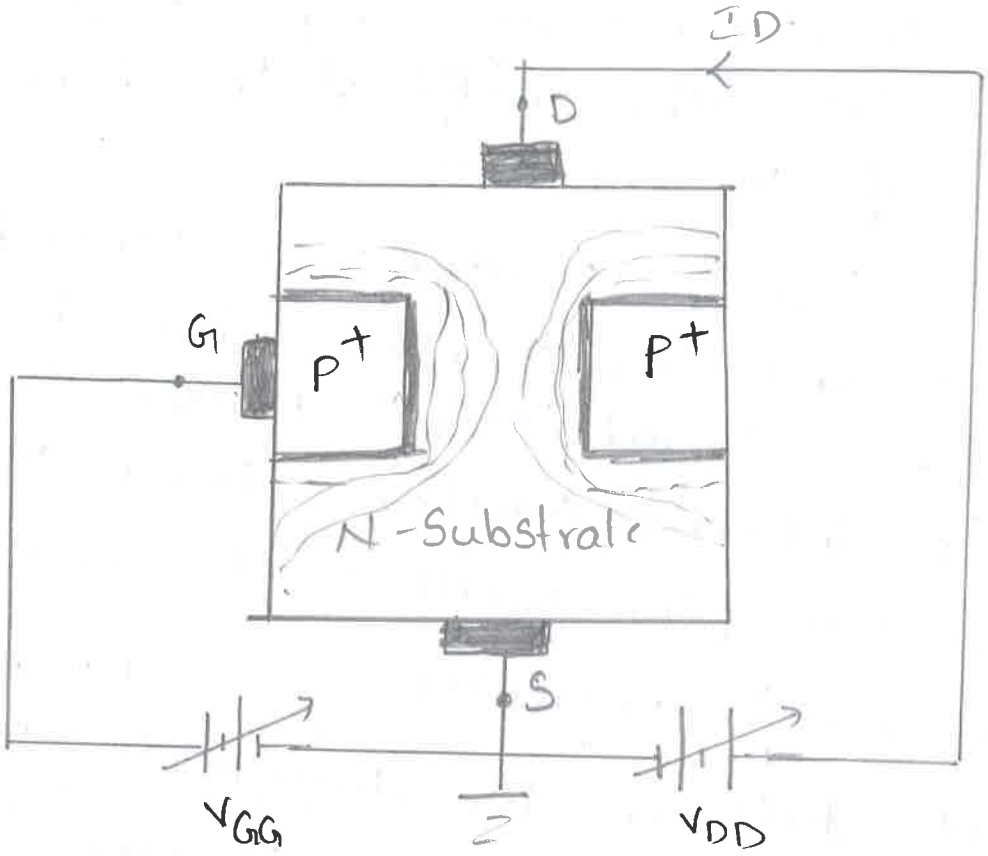
* If $V_{GS} = 0V$, $V_{DS} > 0V$ the width of depletion layer becomes maximum. In this case, the I_D current increases as V_{DS} increases.
* In this case, the drain terminal becomes more negative and the channel width near drain terminal.

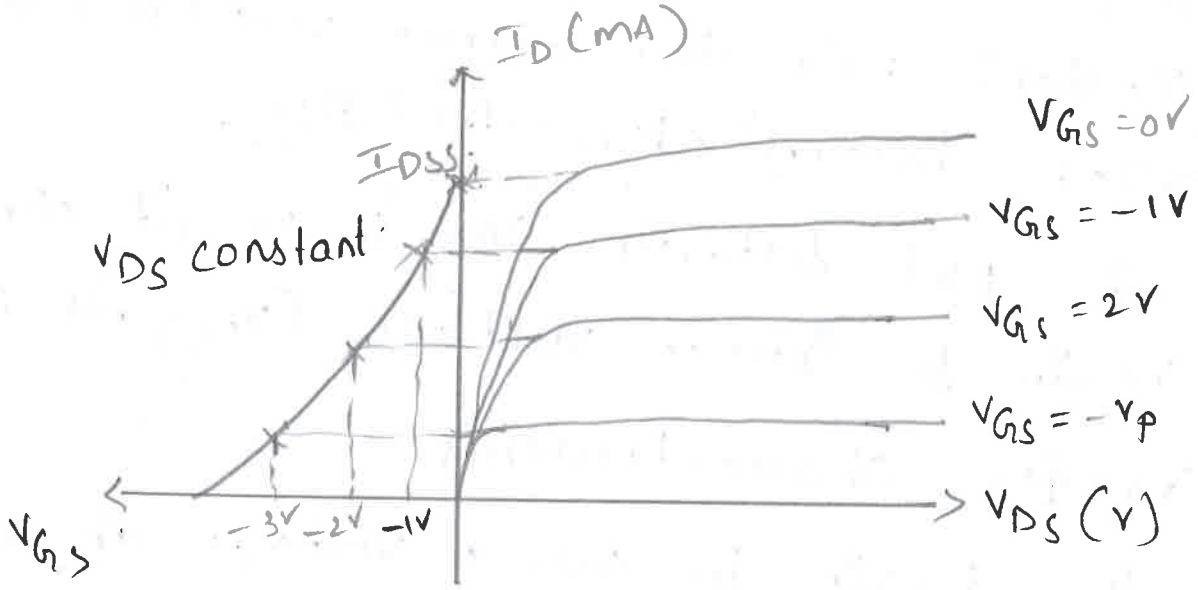
10)a) Differentiate between Enhancement-mode and Depletion-mode MOSFETs [7M]

S.No	Parameter	Enhancement MOSFET	Depletion MOSFET
1.	Operation	Requires a positive gate voltage to conduct	conducts in its natural state and requires no gate voltage
2.	Symbol		
3.	Threshold voltage	positive threshold voltage required	Negative threshold voltage required.
4	Applications	widely used in digital circuits and CMOS technology	less common in digital applications, more in analog circuits
5.	Carrier Type	Majority Carriers are electrons	Majority carriers are holes
6.	Voltage Biasing	Commonly used in NMOS and PMOS transistors	less commonly used in modern CMOS technology.
7.	Circuit design	Requires additional circuitry for pull-up or pull-down resistors	Simplifies circuit design, may not require additional resistors

10)b) Draw and explain the transfer characteristics of N-channel JFET. [7M]

Ans





Case I: If V_{GS} is operated in Reverse bias condition and $V_{DS} = 1V$ then the drain current is in the order of the 1mA.

case-II If V_{GS} is operated in reverse bias condition and $V_{DS} = 2V$ then the drain current I_D is increases from 1mA to 5mA In this case, the width of the channel also increases if V_{DS} increases.

case III : If V_{GS} is operated in reverse bias condition and V_{DS} increases but drain current is almost equal to the case II i.e., it maintains constant drain current. In this case the width of the channel is not much increases.

- The plot between the drain to source voltage (V_{DS}) & the drain current (I_D) at constant gate to source voltage (V_{GS}) is called drain characteristics.
- The plot between V_{GS} & I_D at constant drain to source voltage (V_{DS}) is called transfer characteristics.
- The drain to source voltage at which the width of the channel become constant is called pinchoff voltage (V_p) Sometimes it is same as the maximum voltage.

- The max drain current at which, the maximum drain to source voltage is I_{DSS} (Saturated drain to source current)

→ Modes of operation of JFET:-

(i) In Saturation region it acts as ON Switch

(ii) In cut-off region it acts as OFF switch.

(iii) In breakdown region, drain voltage exceeds maximum.

Verified

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